FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-10185-1E

MEMORY

# CMOS 1M × 4 BIT HYPER PAGE MODE DYNAMIC RAM

# MB81V4405C-60/-70

**CMOS 1,048,576 × 4 BIT Hyper Page Mode Dynamic RAM**



## ■ DESCRIPTION

The Fujitsu MB81V4405C is a fully decoded CMOS Dynamic RAM (DRAM) that contains 4,194,304 memory cells accessible in 4-bit increments. The MB81V4405C features the “hyper page” mode of operation which provides extended valid time for data output and higher speed random access of up to 1,024-bits of data within the same row than the fast page mode. The MB81V4405C DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V4405C is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V4405C is fabricated using silicon gate CMOS and Fujitsu’s advanced four-layer polysilicon process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V4405C are not critical and all inputs are LVTTL compatible.

## ■ ABSOLUTE MAXIMUM RATINGS (See NOTE.)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage at any pin relative to $V_{SS}$ | $V_{IN}$, $V_{OUT}$ | –0.5 to +4.6 | V |
| Voltage of $V_{CC}$ supply relative to $V_{SS}$ | $V_{CC}$ | –0.5 to +4.6 | V |
| Power Dissipation | $P_D$ | 1.0 | W |
| Short Circuit Output Current | $I_{OUT}$ | –50 to +50 | mA |
| Storage Temperature | $T_{STG}$ | –55 to +125 | °C |

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

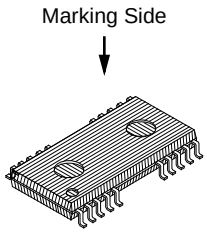
# MB81V4405C-60/MB81V4405C-70

## ■ PRODUCT LINE & FEATURES

| Parameter | | | MB81V4405C-60 | MB81V4405C-70 |
|---|---|---|---|---|
| $\overline{RAS}$ Access Time | | | 60 ns max. | 70 ns max. |
| $\overline{CAS}$ Access Time | | | 15 ns max. | 20 ns max. |
| Address Access Time | | | 30 ns max. | 35 ns max. |
| Random Cycle Time | | | 104 ns min. | 119 ns min. |
| Hyper Page Mode Cycle Time | | | 25 ns min. | 30 ns min. |
| Low Power Dissipation | Operating current | Nomal Mode | 220 mW max. | 195 mW max. |
| | | Hyper Page Mode | 238 mW max. | 198 mW max. |
| | Standby current | | 7.2 mW max. (LVTTL level)/3.6 mW max. (CMOS level) | |

- 1,048,576 words × 4 bit organization
- Silicon gate, CMOS, Advanced-Stacked Capacitor Cell
- All input and output are LVTTL compatible
- 1024 refresh cycles every 16.4 ms
- Self refresh function
- Early write or $\overline{OE}$ controlled write capability
- $\overline{RAS}$-only, $\overline{CAS}$-before-$\overline{RAS}$, or Hidden Refresh
- Hyper page mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance

## ■ PACKAGE



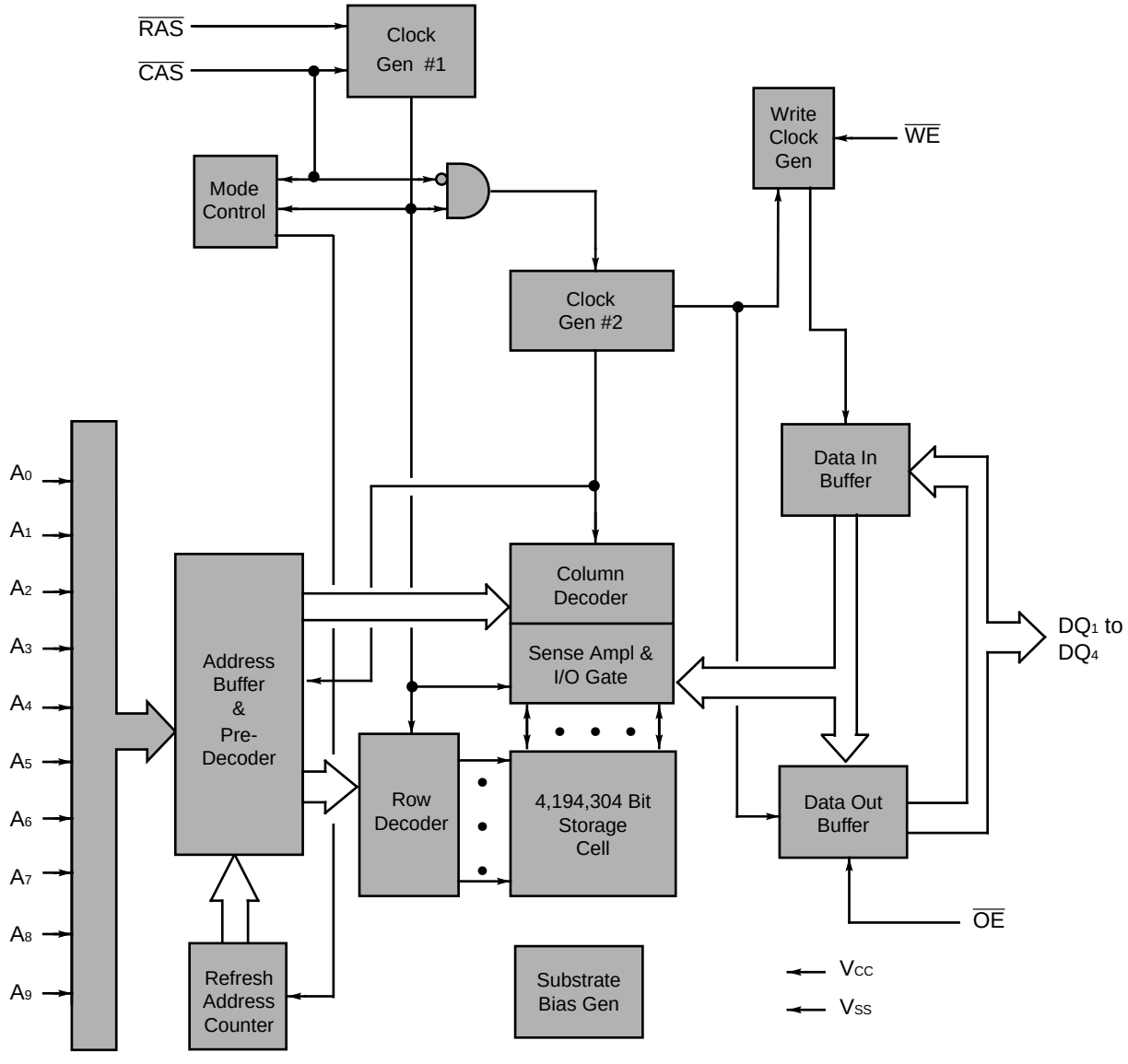

(Normal Bend)
FPT-26P-M01

**Package and Ordering Information**

– 26-pin plastic (300 mil) TSOP-II with normal bend leads, order as MB81V4405C-xxPFTN

# MB81V4405C-60/MB81V4405C-70

**Fig. 1 – MB81V4405C DYNAMIC RAM - BLOCK DIAGRAM**




## ■ CAPACITANCE

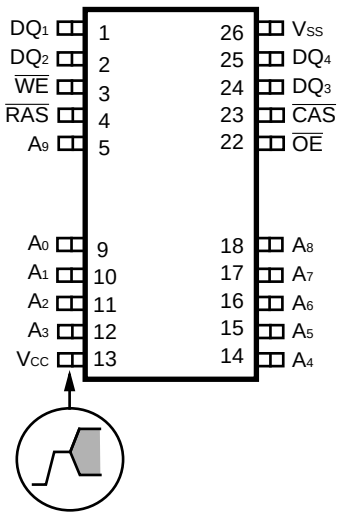
($T_A$ = 25°C, f = 1 MHz)

| Parameter | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Input Capacitance, $A_0$ to $A_9$ | $C_{IN1}$ | — | 5 | pF |
| Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | $C_{IN2}$ | — | 7 | pF |
| Input/Output Capacitance, $DQ_1$ to $DQ_4$ | $C_{DQ}$ | — | 7 | pF |

# MB81V4405C-60/MB81V4405C-70

## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

**26-Pin TSOP:**
(Top View)
<Normal Bend: FPT-26P-M01>




| Designator | Function |
|---|---|
| $DQ_1$ to $DQ_4$ | Data Input/ Output |
| $\overline{WE}$ | Write Enable. |
| $\overline{RAS}$ | Row address strobe. |
| $A_0$ to $A_9$ | Address inputs. |
| $V_{CC}$ | +3.3 volt power supply |
| $\overline{OE}$ | Output enable. |
| $\overline{CAS}$ | Column address strobe. |
| $V_{SS}$ | Circuit ground. |

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Notes | Symbol | Min. | Typ. | Max. | Unit | Ambient Operating Temp. |
|---|---|---|---|---|---|---|---|
| Supply Voltage | 1 | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 0°C to +70°C |
| | | $V_{SS}$ | 0 | 0 | 0 | | |
| Input High Voltage, all inputs | 1 | $V_{IH}$ | 2.0 | — | $V_{CC}$ +0.3 | V | |
| Input Low Voltage, all inputs* | 1 | $V_{IL}$ | –0.3 | — | 0.8 | V | |

* : Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

## ■ FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any four of 4,194,304 cell addresses in the memory matrix. Since only ten address bits are available, the column and row inputs are separately strobed by $\overline{CAS}$ and $\overline{RAS}$ as shown in Figure 5. First, ten row address bits are input on pins $A_0$-through-$A_9$ and latched with the row address strobe ($\overline{RAS}$) then, ten column address bits are input and latched with the column address strobe ($\overline{CAS}$). Both row and column addresses must be stable on or before the falling edge of $\overline{CAS}$ and $\overline{RAS}$, respectively. The address latches are of the flow-through type; thus, address information appearing after $t_{RAH}$ (min.) + $t_T$ is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of $\overline{WE}$. When $\overline{WE}$ is active Low, a write cycle is initiated; when $\overline{WE}$ is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUT

Input data is written into memory in either of three basic ways—an early write cycle, an $\overline{OE}$ (delayed) write cycle, and a read-modify-write cycle. The falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data ($DQ_1$-$DQ_4$) is strobed by $\overline{CAS}$ and the setup/hold times are referenced to $\overline{CAS}$ because $\overline{WE}$ goes Low before $\overline{CAS}$. In a delayed write or a read-modify-write cycle, $\overline{WE}$ goes Low after $\overline{CAS}$; thus, input data is strobed by $\overline{WE}$ and all setup/hold times are referenced to the write-enable signal.

### DATA OUTPUT

The three-state buffers are LVTTL compatible with a fanout of one TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs and High-Z state are obtained under the following conditions:

- $t_{RAC}$ : from the falling edge of $\overline{RAS}$ when $t_{RCD}$ (max.) is satisfied.
- $t_{CAC}$ : from the falling edge of $\overline{CAS}$ when $t_{RCD}$ is greater than $t_{RCD}$ (max.).
- $t_{AA}$ : from column address input when $t_{RAD}$ is greater than $t_{RAD}$ (max.), and $t_{RCD}$ (max.) is satisfied.
- $t_{OEA}$ : from the falling edge of $\overline{OE}$ when $\overline{OE}$ is brought Low after $t_{RAC}$, $t_{CAC}$, or $t_{AA}$.
- $t_{OEZ}$ : from $\overline{OE}$ inactive.
- $t_{OFF}$ : from $\overline{CAS}$ inactive while $\overline{RAS}$ inactive.
- $t_{OFR}$ : from $\overline{RAS}$ inactive while $\overline{CAS}$ inactive.
- $t_{WEZ}$ : from $\overline{WE}$ active while $\overline{CAS}$ inactive.

The data remains valid after either $\overline{OE}$ is inactive, or both $\overline{RAS}$ and $\overline{CAS}$ are inactive, or $\overline{CAS}$ is reactived. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

## HYPER PAGE MODE OF OPERATION

The hyper page mode operation provides faster memory access and lower power dissipation. The hyper page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions, $\overline{RAS}$ is held Low for all contiguous memory cycles in which row addresses are common. For each page of memory (within column address locations), any of 1,024 × 4-bits can be accessed and, when multiple MB81V4405Cs are used, $\overline{CAS}$ is decoded to select the desired memory page. Hyper page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted. Hyper page mode features that output remains valid when $\overline{CAS}$ is inactive until $\overline{CAS}$ is reactivated.

## ■ DC CHARACTERISTICS

**(Recommended operating conditions unless otherwise noted.)** **Notes 3**

| Parameter | | Notes | Symbol | Conditions | Value | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Typ. | Max. | |
| Output high voltage | | 1 | $V_{OH}$ | $I_{OH}$ = –2 mA | 2.4 | — | — | V |
| Output low voltage | | 1 | $V_{OL}$ | $I_{OL}$ = 2 mA | — | — | 0.4 | |
| Input leakage current (Any input) | | | $I_{I(L)}$ | 0 V ≤ $V_{IN}$ ≤ 3.6 V; 3.0 V ≤ $V_{CC}$ ≤ 3.6 V; $V_{SS}$ = 0 V; All other pins not under test = 0 V | –10 | — | 10 | µA |
| Output leakage current | | | $I_{O(L)}$ | 0 V ≤ $V_{OUT}$ ≤ 3.6 V; Data out disabled | –10 | — | 10 | |
| Operating current (Average power supply current) | MB81V4405C-60 | 2 | $I_{CC1}$ | $\overline{RAS}$ & $\overline{CAS}$ cycling; $t_{RC}$ = min. | — | — | 61 | mA |
| | MB81V4405C-70 | | | | | | 54 | |
| Standby current (Power supply current) | LVTTL level | | $I_{CC2}$ | $\overline{RAS}$ = $\overline{CAS}$ = $V_{IH}$ | — | — | 2.0 | mA |
| | CMOS level | | | $\overline{RAS}$ = $\overline{CAS}$ ≥ $V_{CC}$ –0.2 V | | | 1.0 | |
| Refresh current #1 (Average power supply current) | MB81V4405C-60 | 2 | $I_{CC3}$ | $\overline{CAS}$ = $V_{IH}$, $\overline{RAS}$ cycling; $t_{RC}$ = min. | — | — | 61 | mA |
| | MB81V4405C-70 | | | | | | 54 | |
| Hyper page mode current | MB81V4405C-60 | 2 | $I_{CC4}$ | $\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$ cycling; $t_{HPC}$ = min. | — | — | 66 | mA |
| | MB81V4405C-70 | | | | | | 55 | |
| Refresh current #2 (Average power supply current) | MB81V4405C-60 | 2 | $I_{CC5}$ | $\overline{RAS}$ cycling; $\overline{CAS}$-before-$\overline{RAS}$; $t_{RC}$ = min. | — | — | 49 | mA |
| | MB81V4405C-70 | | | | | | 44 | |
| Refresh current #3 (Average power supply current) | MB81V4405C-60 | | $I_{CC9}$ | $\overline{RAS}$ = $\overline{CAS}$ ≤ 0.2 V Self refresh | — | — | 1000 | µA |
| | MB81V4405C-70 | | | | | | 1000 | |

# MB81V4405C-60/MB81V4405C-70

## ■ AC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.)** **Notes 3, 4, 5**

| No. | Parameter | Notes | Symbol | MB81V4405C-60 | | MB81V4405C-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 1 | Time Between Refresh | | $t_{REF}$ | — | 16.4 | — | 16.4 | ms |
| 2 | Random Read/Write Cycle Time | | $t_{RC}$ | 104 | — | 119 | — | ns |
| 3 | Read-Modify-Write Cycle Time | | $t_{RWC}$ | 138 | — | 156 | — | ns |
| 4 | Access Time from $\overline{RAS}$ | 6, 9 | $t_{RAC}$ | — | 60 | — | 70 | ns |
| 5 | Access Time from $\overline{CAS}$ | 7, 9 | $t_{CAC}$ | — | 15 | — | 20 | ns |
| 6 | Column Address Access Time | 8, 9 | $t_{AA}$ | — | 30 | — | 35 | ns |
| 7 | Output Hold Time | | $t_{OH}$ | 5 | — | 5 | — | ns |
| 8 | Output Hold Time from $\overline{CAS}$ | | $t_{OHC}$ | 5 | — | 5 | — | ns |
| 9 | Output Buffer Turn On Delay Time | | $t_{ON}$ | 0 | — | 0 | — | ns |
| 10 | Output Buffer Turn Off Delay Time | 10 | $t_{OFF}$ | — | 15 | — | 15 | ns |
| 11 | Output Buffer Turn Off Delay Time from $\overline{RAS}$ | | $t_{OFR}$ | — | 15 | — | 15 | ns |
| 12 | Output Buffer Turn Off Delay Time from $\overline{WE}$ | | $t_{WEZ}$ | — | 15 | — | 15 | ns |
| 13 | Transition Time | | $t_T$ | 1 | 50 | 1 | 50 | ns |
| 14 | $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 40 | — | 45 | — | ns |
| 15 | $\overline{RAS}$ Pulse Width | | $t_{RAS}$ | 60 | 100000 | 70 | 100000 | ns |
| 16 | $\overline{RAS}$ Hold Time | | $t_{RSH}$ | 15 | — | 20 | — | ns |
| 17 | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 21 | $t_{CRP}$ | 0 | — | 0 | — | ns |
| 18 | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | 11, 12, 22 | $t_{RCD}$ | 14 | 45 | 14 | 50 | ns |
| 19 | $\overline{CAS}$ Pulse Width | | $t_{CAS}$ | 10 | 10000 | 10 | 10000 | ns |
| 20 | $\overline{CAS}$ Hold Time | | $t_{CSH}$ | 40 | — | 50 | — | ns |
| 21 | $\overline{CAS}$ Precharge Time (Normal) | 19 | $t_{CPN}$ | 10 | — | 10 | — | ns |
| 22 | Row Address Set Up Time | | $t_{ASR}$ | 0 | — | 0 | — | ns |
| 23 | Row Address Hold Time | | $t_{RAH}$ | 10 | — | 10 | — | ns |
| 24 | Column Address Set Up Time | | $t_{ASC}$ | 0 | — | 0 | — | ns |
| 25 | Column Address Hold Time | | $t_{CAH}$ | 10 | — | 10 | — | ns |
| 26 | $\overline{RAS}$ to Column Address Delay Time | 13 | $t_{RAD}$ | 12 | 30 | 12 | 35 | ns |
| 27 | Column Address to $\overline{RAS}$ Lead Time | | $t_{RAL}$ | 30 | — | 35 | — | ns |
| 28 | Column Address to $\overline{CAS}$ Lead Time | | $t_{CAL}$ | 23 | — | 28 | — | ns |
| 29 | Read Command Set Up Time | | $t_{RCS}$ | 0 | — | 0 | — | ns |
| 30 | Read Command Hold Time Referenced to $\overline{RAS}$ | 14 | $t_{RRH}$ | 0 | — | 0 | — | ns |

*(Continued)*

## ■ AC CHARACTERISTICS (Continued)

**(At recommended operating conditions unless otherwise noted.)** **Notes 3, 4, 5**

| No. | Parameter | Notes | Symbol | MB81V4405C-60 | | MB81V4405C-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 31 | Read Command Hold Time Referenced to $\overline{CAS}$ | 14 | $t_{RCH}$ | 0 | — | 0 | — | ns |
| 32 | Write Command Set Up Time | 15 | $t_{WCS}$ | 0 | — | 0 | — | ns |
| 33 | Write Command Hold Time | | $t_{WCH}$ | 10 | — | 10 | — | ns |
| 34 | $\overline{WE}$ Pulse Width | | $t_{WP}$ | 10 | — | 10 | — | ns |
| 35 | Write Command to $\overline{RAS}$ Lead Time | | $t_{RWL}$ | 15 | — | 18 | — | ns |
| 36 | Write Command to $\overline{CAS}$ Lead Time | | $t_{CWL}$ | 10 | — | 10 | — | ns |
| 37 | DIN Set Up Time | | $t_{DS}$ | 0 | — | 0 | — | ns |
| 38 | DIN Hold Time | | $t_{DH}$ | 10 | — | 10 | — | ns |
| 39 | $\overline{RAS}$ to $\overline{WE}$ Delay Time | | $t_{RWD}$ | 77 | — | 87 | — | ns |
| 40 | $\overline{CAS}$ to $\overline{WE}$ Delay Time | | $t_{CWD}$ | 32 | — | 37 | — | ns |
| 41 | Column Address to $\overline{WE}$ Delay Time | | $t_{AWD}$ | 47 | — | 52 | — | ns |
| 42 | $\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles) | | $t_{RPC}$ | 5 | — | 5 | — | ns |
| 43 | $\overline{CAS}$ Set Up Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh | | $t_{CSR}$ | 0 | — | 0 | — | ns |
| 44 | $\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Refresh | | $t_{CHR}$ | 10 | — | 10 | — | ns |
| 45 | $\overline{WE}$ Set Up Time from $\overline{RAS}$ | 20 | $t_{WSR}$ | 0 | — | 0 | — | ns |
| 46 | $\overline{WE}$ Hold Time from $\overline{RAS}$ | 20 | $t_{WHR}$ | 10 | — | 10 | — | ns |
| 47 | Access Time from $\overline{OE}$ | 9 | $t_{OEA}$ | — | 15 | — | 20 | ns |
| 48 | Output Buffer Turn Off Delay from $\overline{OE}$ | 10 | $t_{OEZ}$ | — | 15 | — | 15 | ns |
| 49 | $\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data | | $t_{OEL}$ | 10 | — | 10 | — | ns |
| 50 | $\overline{OE}$ to $\overline{CAS}$ Lead Time | | $t_{COL}$ | 5 | — | 5 | — | ns |
| 51 | $\overline{OE}$ Hold Time Referenced to $\overline{WE}$ | 16 | $t_{OEH}$ | 0 | — | 0 | — | ns |
| 52 | $\overline{OE}$ to Data In Delay Time | | $t_{OED}$ | 15 | — | 15 | — | ns |
| 53 | DIN to $\overline{CAS}$ Delay Time | 17 | $t_{DZC}$ | 0 | — | 0 | — | ns |
| 54 | DIN to $\overline{OE}$ Delay Time | 17 | $t_{DZO}$ | 0 | — | 0 | — | ns |
| 55 | $\overline{OE}$ Precharge Time | | $t_{OEP}$ | 10 | — | 10 | — | ns |
| 56 | $\overline{OE}$ Hold Time Referenced to $\overline{CAS}$ | | $t_{OECH}$ | 10 | — | 10 | — | ns |
| 57 | $\overline{WE}$ Precharge Time | | $t_{WPZ}$ | 10 | — | 10 | — | ns |
| 58 | $\overline{WE}$ to Data In Delay Time | | $t_{WED}$ | 15 | — | 15 | — | ns |
| 59 | $\overline{RAS}$ to Data In Delay Time | | $t_{RDD}$ | 15 | — | 15 | — | ns |
| 60 | $\overline{CAS}$ to Data In Delay Time | | $t_{CDD}$ | 15 | — | 15 | — | ns |

*(Continued)*

## ■ AC CHARACTERISTICS (Continued)

**(At recommended operating conditions unless otherwise noted.)** **Notes 3, 4, 5**

| No. | Parameter | Notes | Symbol | MB81V4405C-60 | | MB81V4405C-70 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | |
| 61 | $\overline{RAS}$ to Columunn Address Hold Time | | $t_{AR}$ | 26 | — | 26 | — | ns |
| 62 | Write Command Hold Time Referenced to $\overline{RAS}$ | | $t_{WCR}$ | 24 | — | 24 | — | ns |
| 63 | Data Input Hold Time Referenced to $\overline{RAS}$ | | $t_{DHR}$ | 24 | — | 24 | — | ns |
| 64 | Hyper Page Mode Read/Write Cycle Time | | $t_{HPC}$ | 25 | — | 30 | — | ns |
| 65 | Hyper Page Mode Read-Modify-Write Cycle Time | | $t_{HPRWC}$ | 66 | — | 71 | — | ns |
| 66 | Access Time from $\overline{CAS}$ Precharge | 9, 18 | $t_{CPA}$ | — | 35 | — | 40 | ns |
| 67 | Hyper Page Mode $\overline{CAS}$ Precharge Time | | $t_{CP}$ | 10 | — | 10 | — | ns |
| 68 | Hyper Page Mode $\overline{RAS}$ Pulse Width | | $t_{RASP}$ | — | 200000 | — | 200000 | ns |
| 69 | Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | | $t_{RHCP}$ | 35 | — | 40 | — | ns |
| 70 | Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time | | $t_{CPWD}$ | 52 | — | 57 | — | ns |

Notes:
1. Referenced to $V_{SS}$.
2. $I_{CC}$ depends on the output load conditions and cycle rates; The specified values are obtained with the output open.
   $I_{CC}$ depends on the number of address change as $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
   $I_{CC1}$, $I_{CC3}$ and $I_{CC5}$ are specified at one time of address change during $\overline{RAS} = V_{IL}$ and $\overline{CAS} = V_{IH}$.
   $I_{CC4}$ is specified at one time of address change during one Page cycle.
3. An Initial pause ($\overline{RAS} = \overline{CAS} = V_{IH}$) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC characteristics assume $t_T$ = 2 ns.
5. $V_{IH}$ (min.) and $V_{IL}$ (max.) are reference levels for measuring timing of input signals. Also transition times are measured between $V_{IH}$ (min.) and $V_{IL}$ (max.).
6. Assumes that $t_{RCD} \leq t_{RCD}$ (max.), $t_{RAD} \leq t_{RAD}$ (max.). If $t_{RCD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ will be increased by the amount that $t_{RCD}$ exceeds the value shown. Refer to Fig. 2 and 3.
7. If $t_{RCD} \geq t_{RCD}$ (max.), $t_{RAD} \geq t_{RAD}$ (max.), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is $t_{CAC}$.
8. If $t_{RAD} \geq t_{RAD}$ (max.) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is $t_{AA}$.
9. Measured with a load equivalent to one TTL loads and 100 pF.
10. $t_{OFF}$ and $t_{OEZ}$ is specified that output buffer change to high impedance state.
11. Operation within the $t_{RCD}$ (max.) limit ensures that $t_{RAC}$ (max.) can be met. $t_{RCD}$ (max.) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max.) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.
12. $t_{RCD}$ (min.) = $t_{RAH}$ (min.) + 2$t_T$ + $t_{ASC}$ (min.).
13. Operation within the $t_{RAD}$ (max.) limit ensures that $t_{RAC}$ (max.) can be met. $t_{RAD}$ (max.) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max.) limit, access time is controlled exclusively by $t_{CAC}$ or $t_{AA}$.
14. Either $t_{RRH}$ or $t_{RCH}$ must be satisfied for a read cycle.
15. $t_{WCS}$ is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min.) the data output pin will remain High-Z state through entire cycle.
16. Assumes that $t_{WCS} < t_{WCS}$ (min.).
17. Either $t_{DZC}$ or $t_{DZO}$ must be satisfied.
18. $t_{CPA}$ is access time from the selection of a new column address (that is caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if $t_{CP}$ is long, $t_{CPA}$ is longer than $t_{CPA}$ (max.) as shown in Fig. 4.
19. Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh.
20. Assumes that Test mode function.
21. The last $\overline{CAS}$ rising edge.
22. The first $\overline{CAS}$ falling edge.

# MB81V4405C-60/MB81V4405C-70

**Fig. 2 – $t_{RAC}$ vs. $t_{RCD}$**

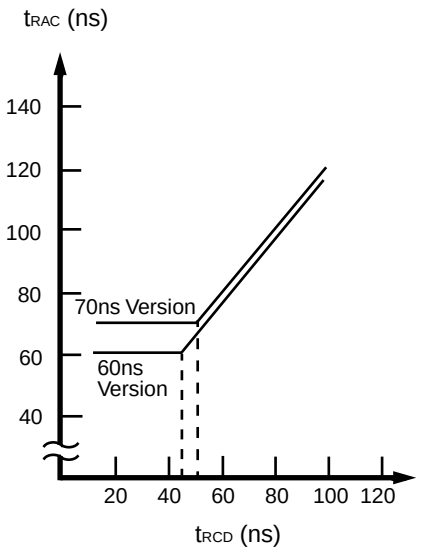



**Fig. 3 – $t_{RAC}$ vs. $t_{RAD}$**

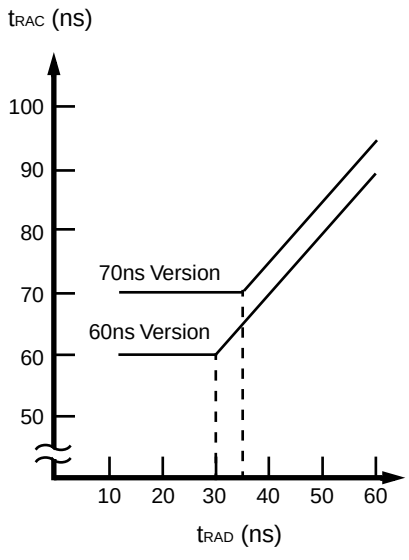
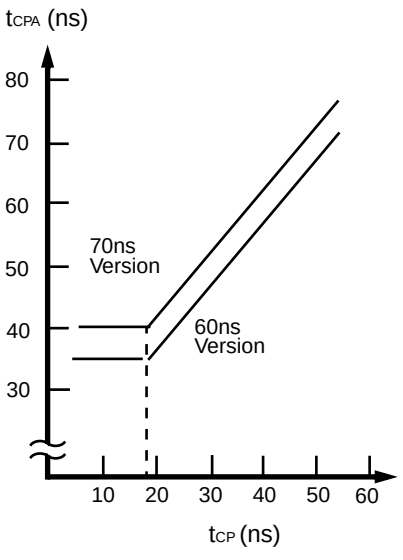



**Fig. 4 – $t_{CPA}$ vs. $t_{CP}$**




## ■ FUNCTIONAL TRUTH TABLE

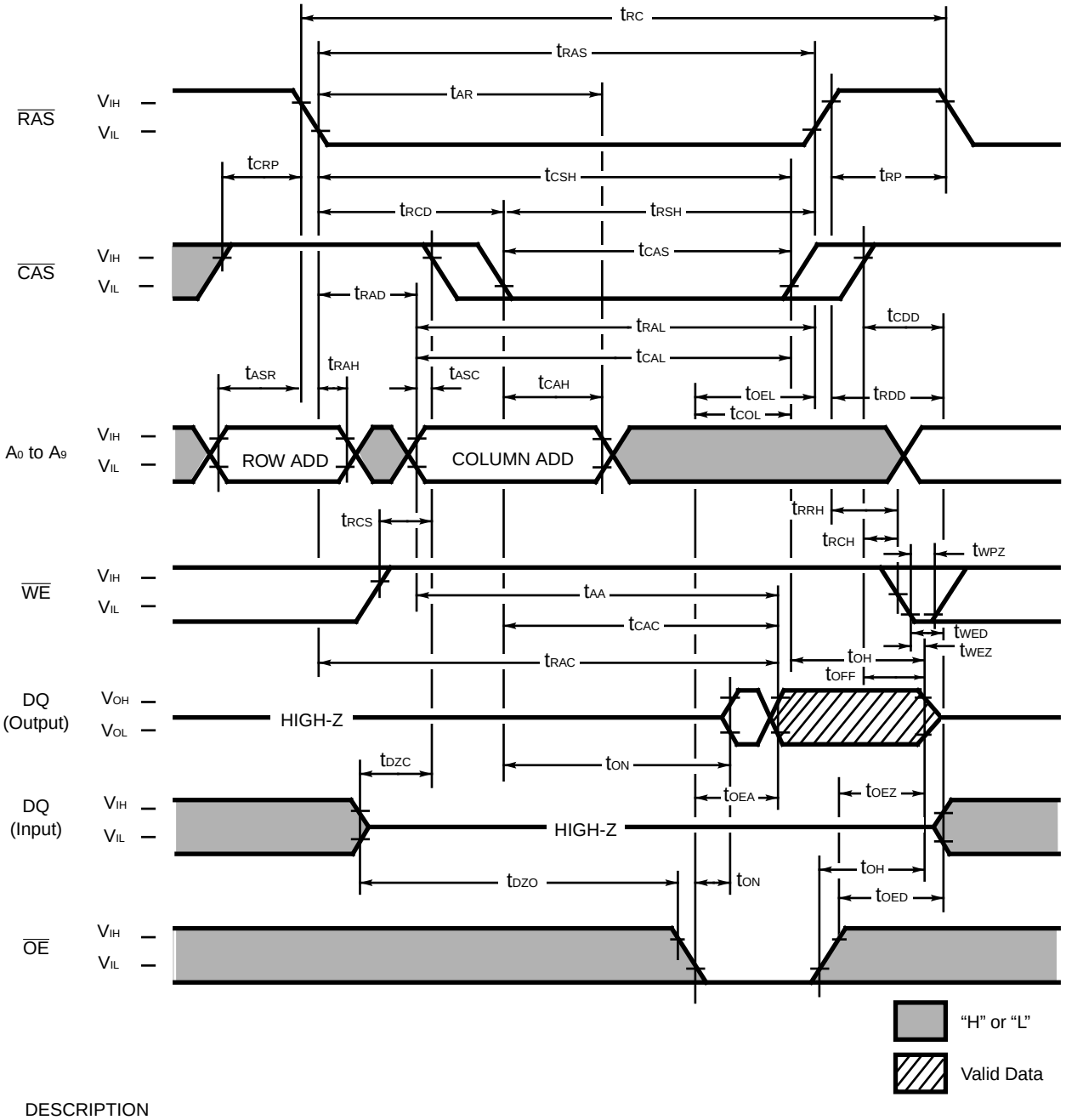
| Operation Mode | Clock Input | | | | Address | | Input Data | | Refresh | Note |
|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | $\overline{OE}$ | Row | Column | Input | Output | | |
| Standby | H | H | X | X | — | — | — | High-Z | — | |
| Read Cycle | L | L | H | L | Valid | Valid | — | Valid | Yes* | $t_{RCS} \geq t_{RCS}$ (min.) |
| Write Cycle (Early Write) | L | L | L | X | Valid | Valid | Valid | High-Z | Yes* | $t_{WCS} \geq t_{WCS}$ (min.) |
| Read-Modify-Write Cycle | L | L | H→L | L→H | Valid | Valid | Valid | Valid | Yes* | $t_{CWD} \geq t_{CWD}$ (min.) |
| $\overline{RAS}$-only Refresh Cycle | L | H | X | X | Valid | — | — | High-Z | Yes | |
| $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle | L | L | H | X | — | — | — | High-Z | Yes | $t_{CSR} \geq t_{CSR}$ (min.) |
| Hidden Refresh Cycle | H→L | L | H | L | — | — | — | Valid | Yes | Previous data is kept |
| Test mode Set Cycle (CBR) | L | L | L | X | — | — | — | High-Z | Yes | $t_{CSR} \geq t_{CSR}$ (min.) $t_{WSR} \geq t_{WSR}$ (min.) |
| Test mode Set Cycle (Hidden) | H→L | L | L | X | — | — | — | Valid | Yes | $t_{CSR} \geq t_{CSR}$ (min.) $t_{WSR} \geq t_{WSR}$ (min.) |

X; “H” or “L”

*; It is impossible in Hyper Page Mode.

# MB81V4405C-60/MB81V4405C-70

**Fig. 5 – READ CYCLE**




DESCRIPTION

To implement a read operation, a valid address is latched by the $\overline{RAS}$ and $\overline{CAS}$ address strobes and with $\overline{WE}$ set to a High level and $\overline{OE}$ set to a Low level, the output is valid once the memory access time has elapsed. The access time is determined by $\overline{RAS}$($t_{RAC}$), $\overline{CAS}$ ($t_{CAC}$), $\overline{OE}$ ($t_{OEA}$) or column addresses ($t_{AA}$) under the following conditions:

If $t_{RCD} > t_{RCD}$ (max.), access time = $t_{CAC}$.

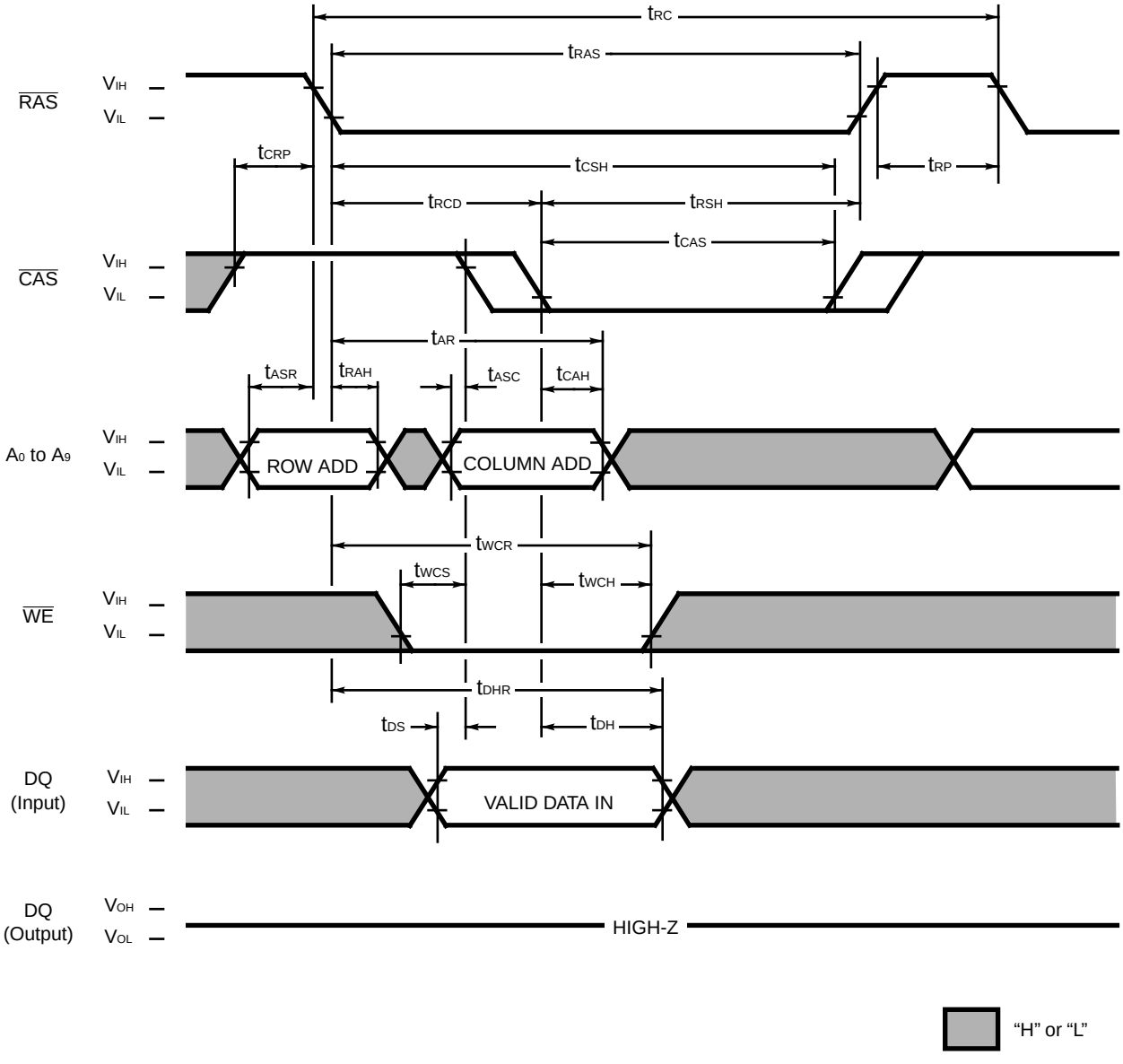
If $t_{RAD} > t_{RAD}$ (max.), access time = $t_{AA}$.

If $\overline{OE}$ is brought Low after $t_{RAC}$, $t_{CAC}$, or $t_{AA}$ (whichever occurs later), access time = $t_{OEA}$.

However, if either $\overline{OE}$ or both $\overline{RAS}$ and $\overline{CAS}$ or $\overline{OE}$ goes High, the output returns to a high-impedance state after $t_{OH}$ is satisfied.

# MB81V4405C-60/MB81V4405C-70

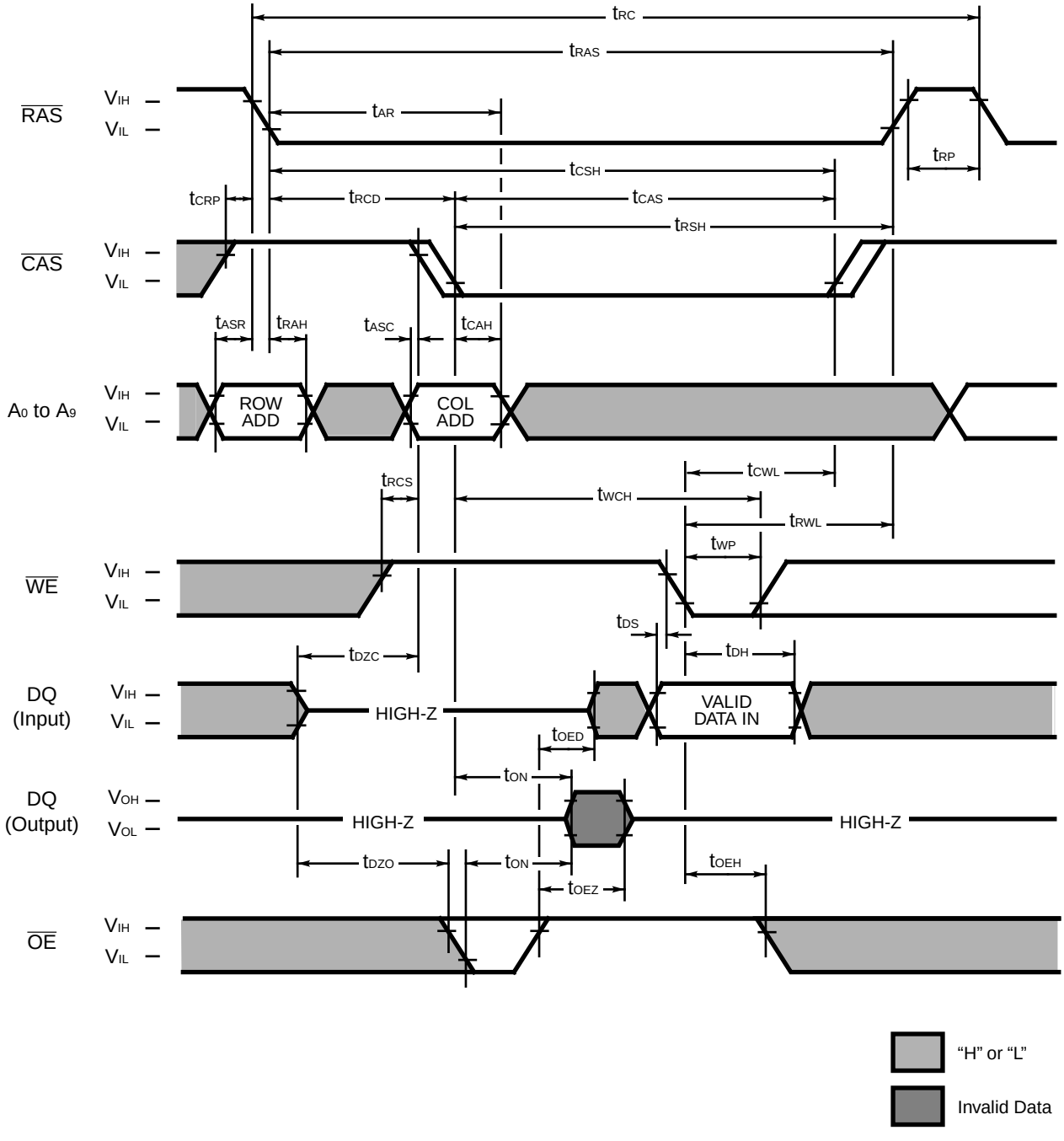
**Fig. 6 – EARLY WRITE CYCLE**




DESCRIPTION

A write cycle is similar to a read cycle except $\overline{WE}$ is set to a Low state and OE is a "H" or "L" signal. A write cycle can be implemented in either of three ways–early write, delayed write, or read-modify-write. During all write cycles, timing parameters $t_{RWL}$, $t_{CWL}$, $t_{RAL}$ and $t_{CAL}$ must be satisfied. In the early write cycle shown above $t_{WCS}$ satisfied, data on the DQ pins are latched with the falling edge of CAS and written into memory.

**Fig. 7 – DELAYED WRITE CYCLE ($\overline{OE}$ CONTROLLED)**

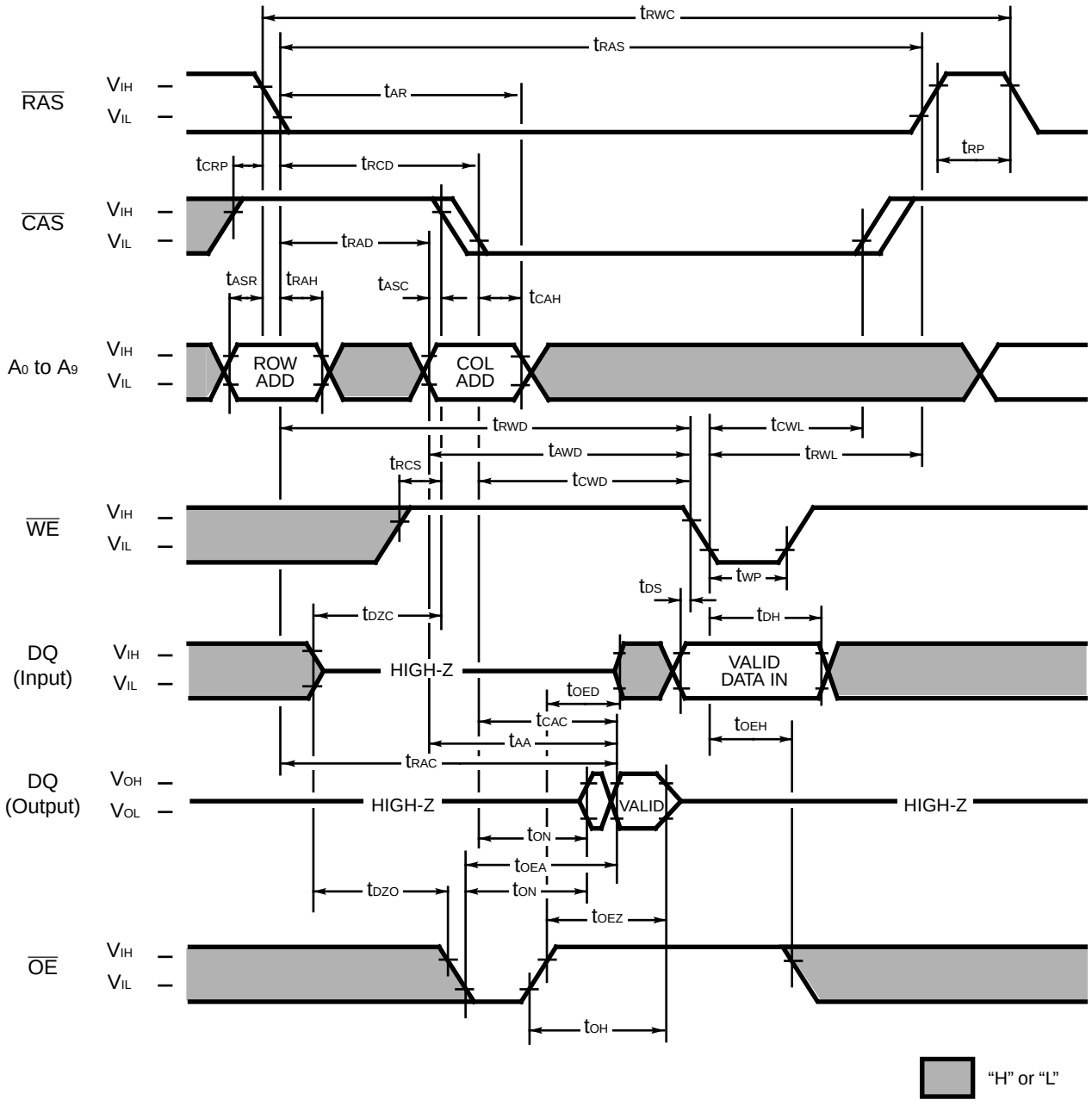



DESCRIPTION

In the delayed write cycle, $t_{WCS}$ is not satisfied; thus, the data on the DQ pins are latched with the falling edge of $\overline{WE}$ and written into memory. The Output Enable ($\overline{OE}$) signal must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

# MB81V4405C-60/MB81V4405C-70

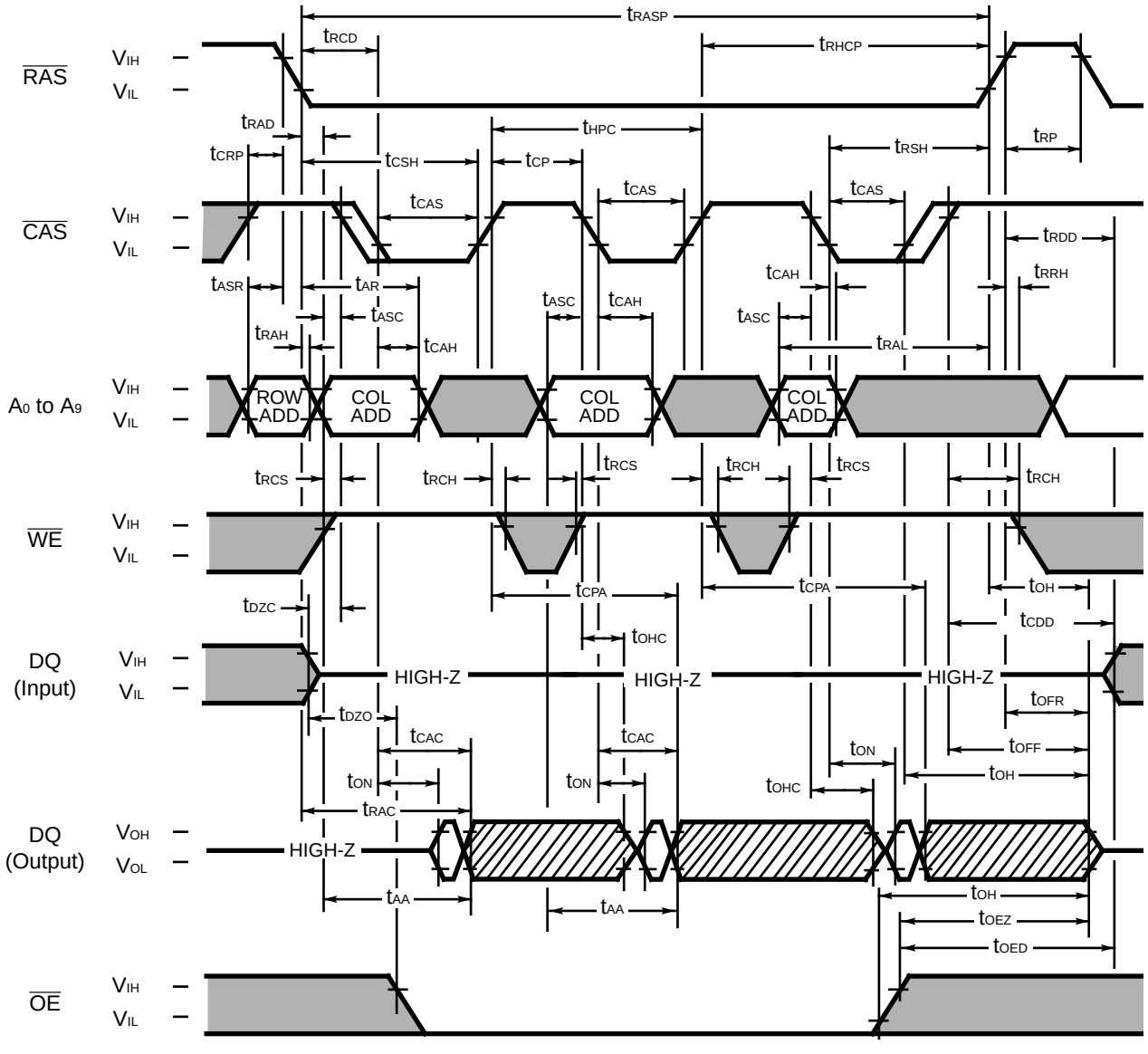
**Fig. 8 – READ-MODIFY-WRITE CYCLE**




DESCRIPTION

The read-modify-write cycle is executed by changing $\overline{WE}$ from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, $\overline{OE}$ must be changed from Low to High after the memory access time.

**Fig. 9 – HYPER PAGE MODE READ CYCLE**




During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

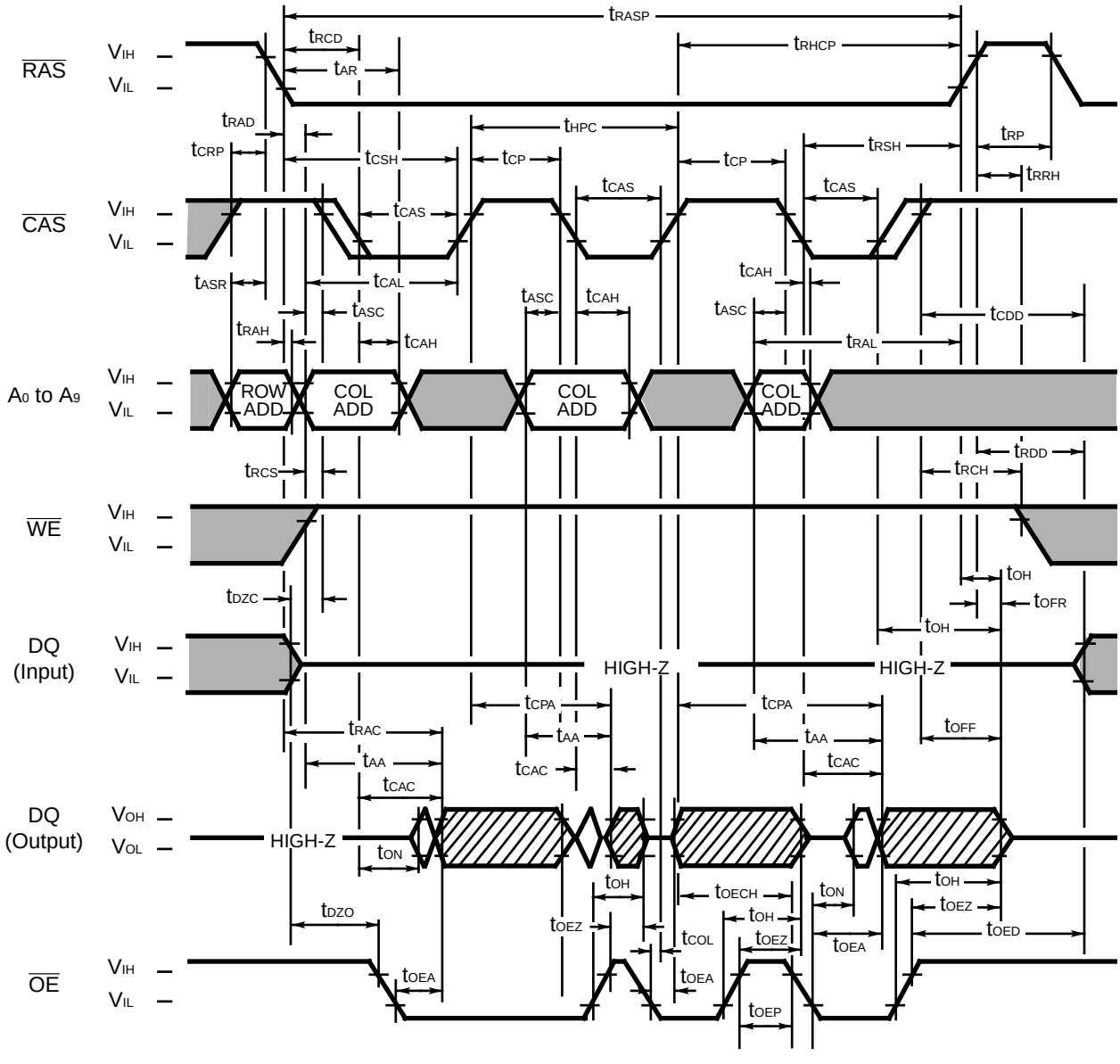
Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level during all successive memory cycles in which the row address is latched. The access time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, whichever one is the latest in occurring.

# MB81V4405C-60/MB81V4405C-70

**Fig. 10 – HYPER PAGE MODE READ CYCLE ($\overline{OE}$ CONTROLLED)**




During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

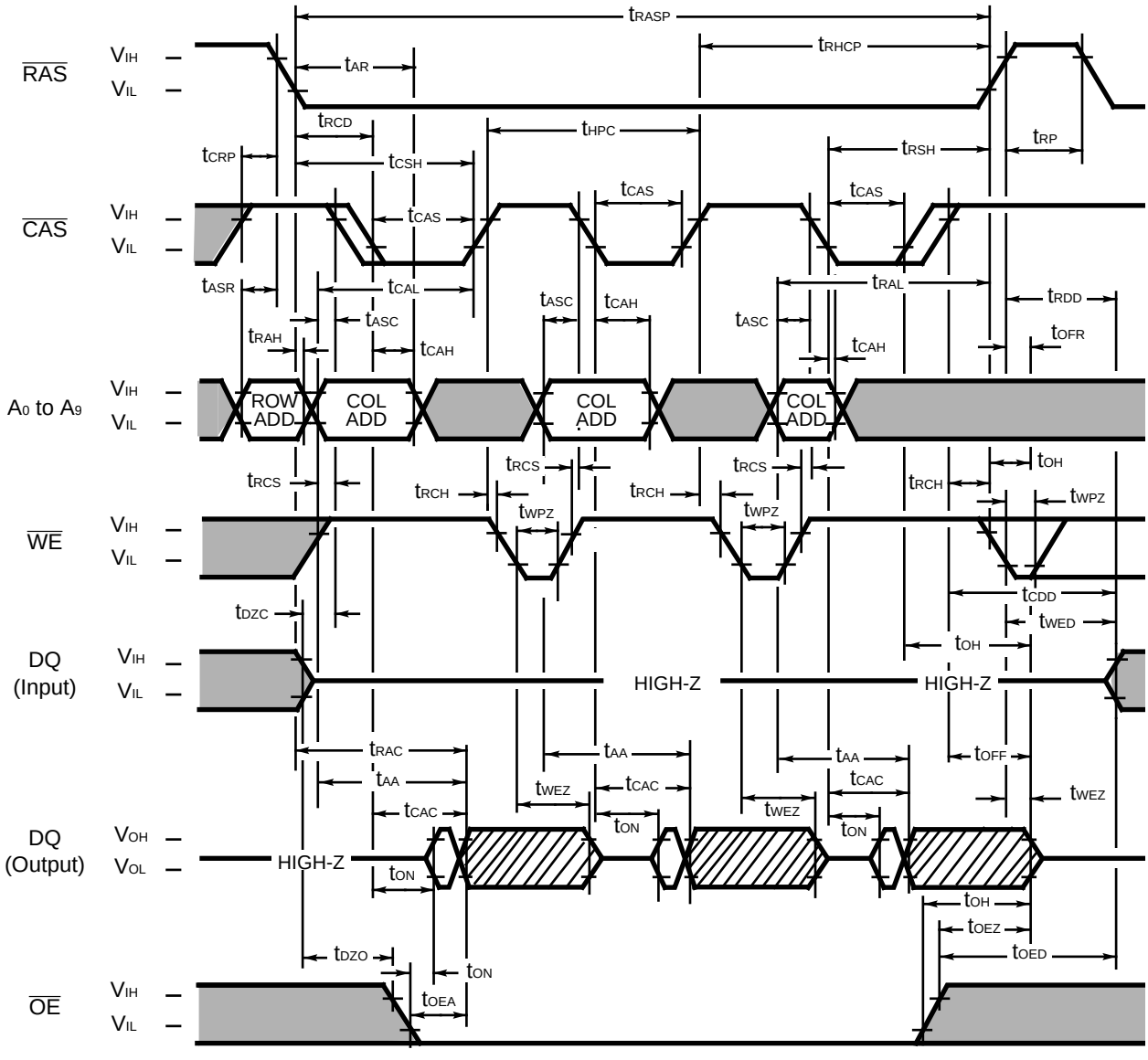
Valid Data

DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The access time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, whichever one is the latest in occurring.

To obtain a high impedance state, set $\overline{OE}$ or both $\overline{RAS}$ and $\overline{CAS}$ going high level.

**Fig. 11 – HYPER PAGE MODE READ CYCLE ($\overline{WE}$ CONTROLLED)**




During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

Valid Data

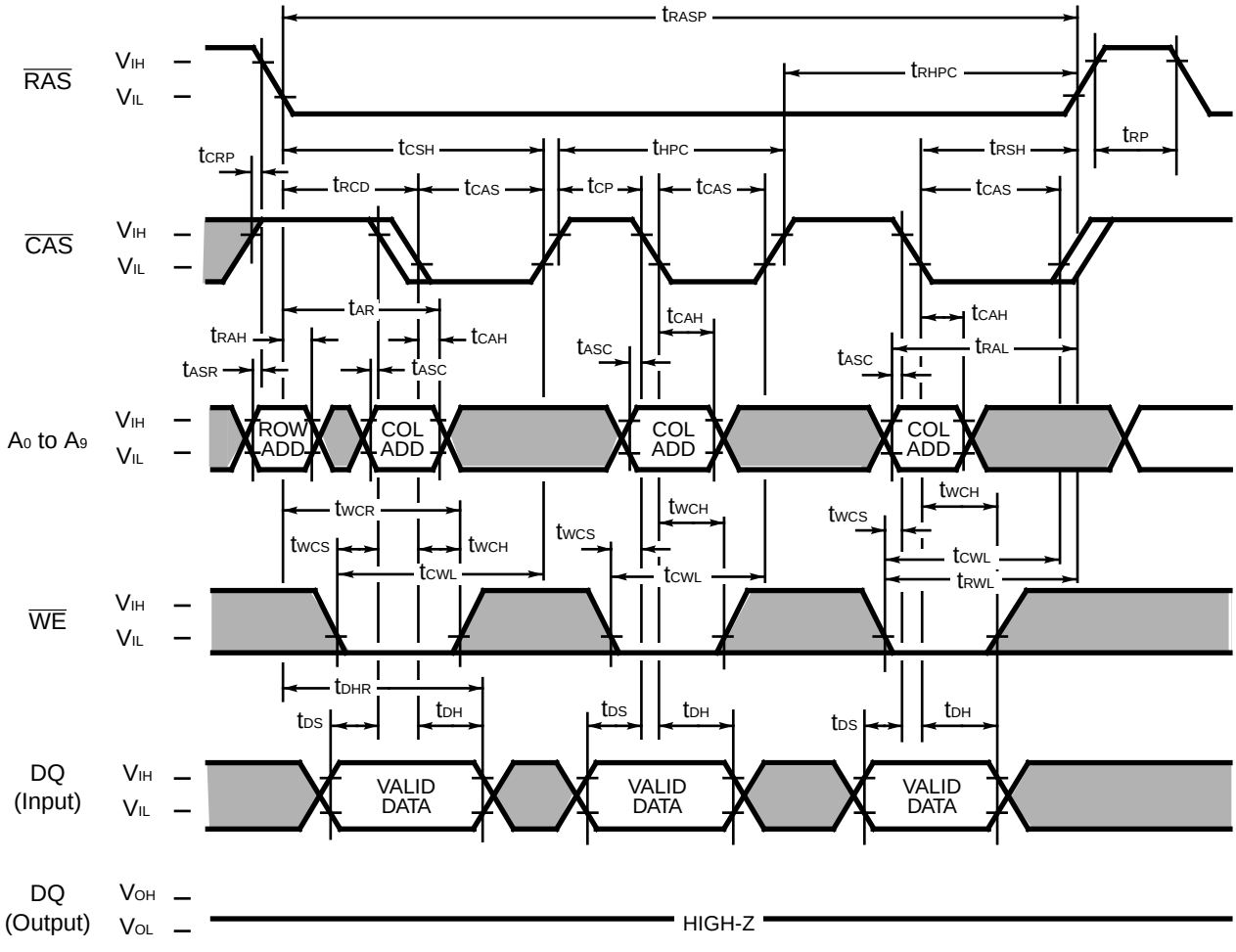
DESCRIPTION

The hyper page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining $\overline{RAS}$ at a Low level and $\overline{WE}$ at a High level during all successive memory cycles in which the row address is latched. The address time is determined by $t_{CAC}$, $t_{AA}$, $t_{CPA}$, or $t_{OEA}$, whichever one is the latest in occurring.

To obtain a high impedance state, confirm either of the following conditions, $\overline{OE}$ set to a high level or $\overline{WE}$ set to a low level after $\overline{CAS}$ set to a high level or $\overline{RAS}$ and $\overline{CAS}$ set to a high level.

# MB81V4405C-60/MB81V4405C-70

**Fig. 12 – HYPER PAGE MODE EARLY WRITE CYCLE**



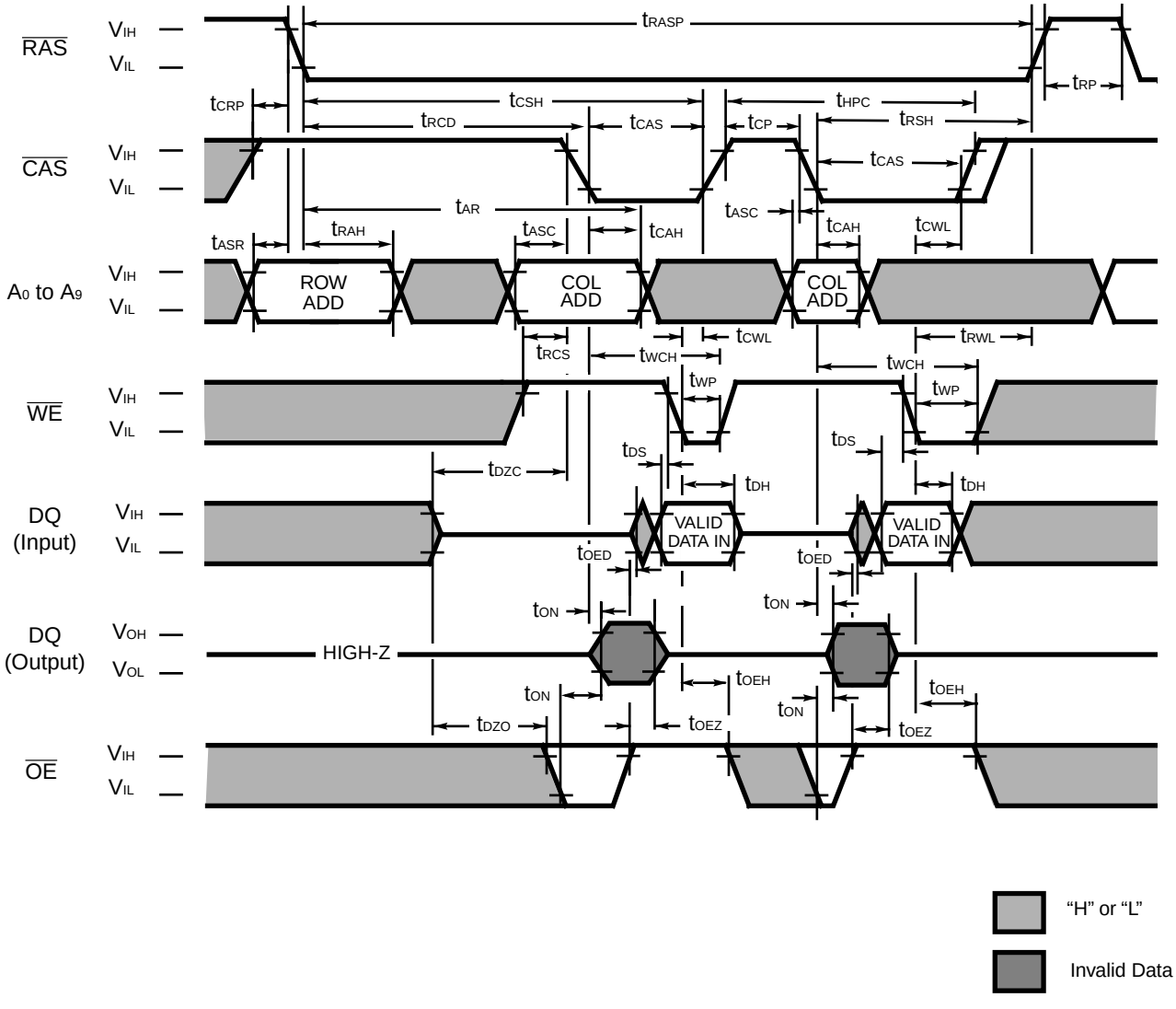

During one cycle is achieved, the input/output timing apply the same manner as the former cycle.

"H" or "L"

DESCRIPTION

The hyper page mode early write cycle is executed in the same manner as the hyper page mode read cycle except $\overline{WE}$ is set to a low state and $\overline{OE}$ is a "H" or "L" signal. Data appearing on the DQ pins is latched on the falling edge of $\overline{CAS}$ and the data is written into the memory. During the hyper page mode write cycle, including the delayed ($\overline{OE}$) write and read-modify-write cycles, $t_{CWL}$ must be satisfied.

**Fig. 13 – HYPER PAGE MODE DELAYED WRITE CYCLE ($\overline{OE}$ CONTROLLED)**

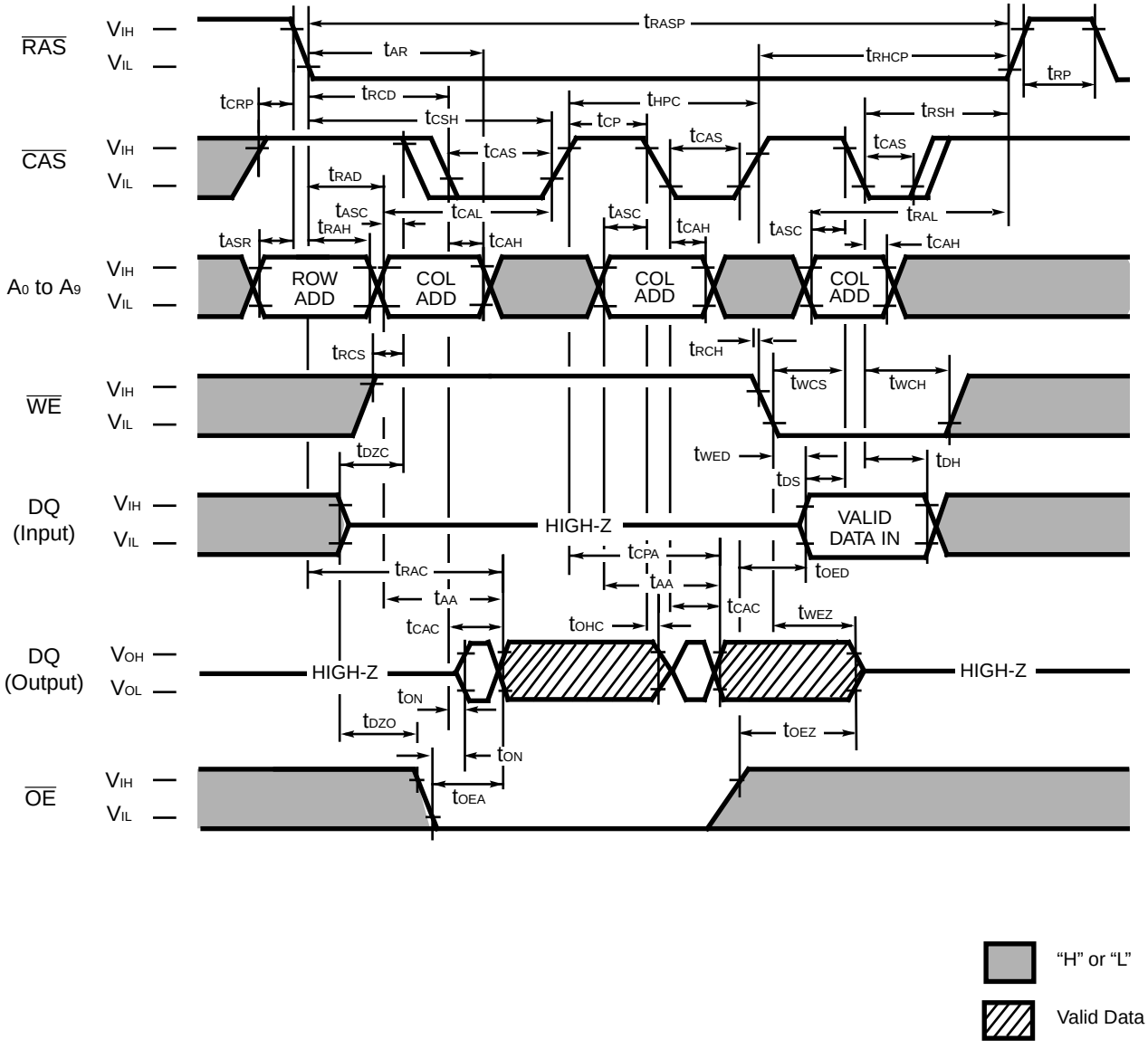



DESCRIPTION

The hyper page mode delayed write cycle is executed in the same manner as the hyper page mode early write cycle except for the states of $\overline{WE}$ and $\overline{OE}$. Input data on the DQ pins are latched on the falling edge of $\overline{WE}$ and written into memory. In the hyper page mode delayed write cycle, $\overline{OE}$ must be changed from Low to High before $\overline{WE}$ goes Low ($t_{OED} + t_T + t_{DS}$).

# MB81V4405C-60/MB81V4405C-70

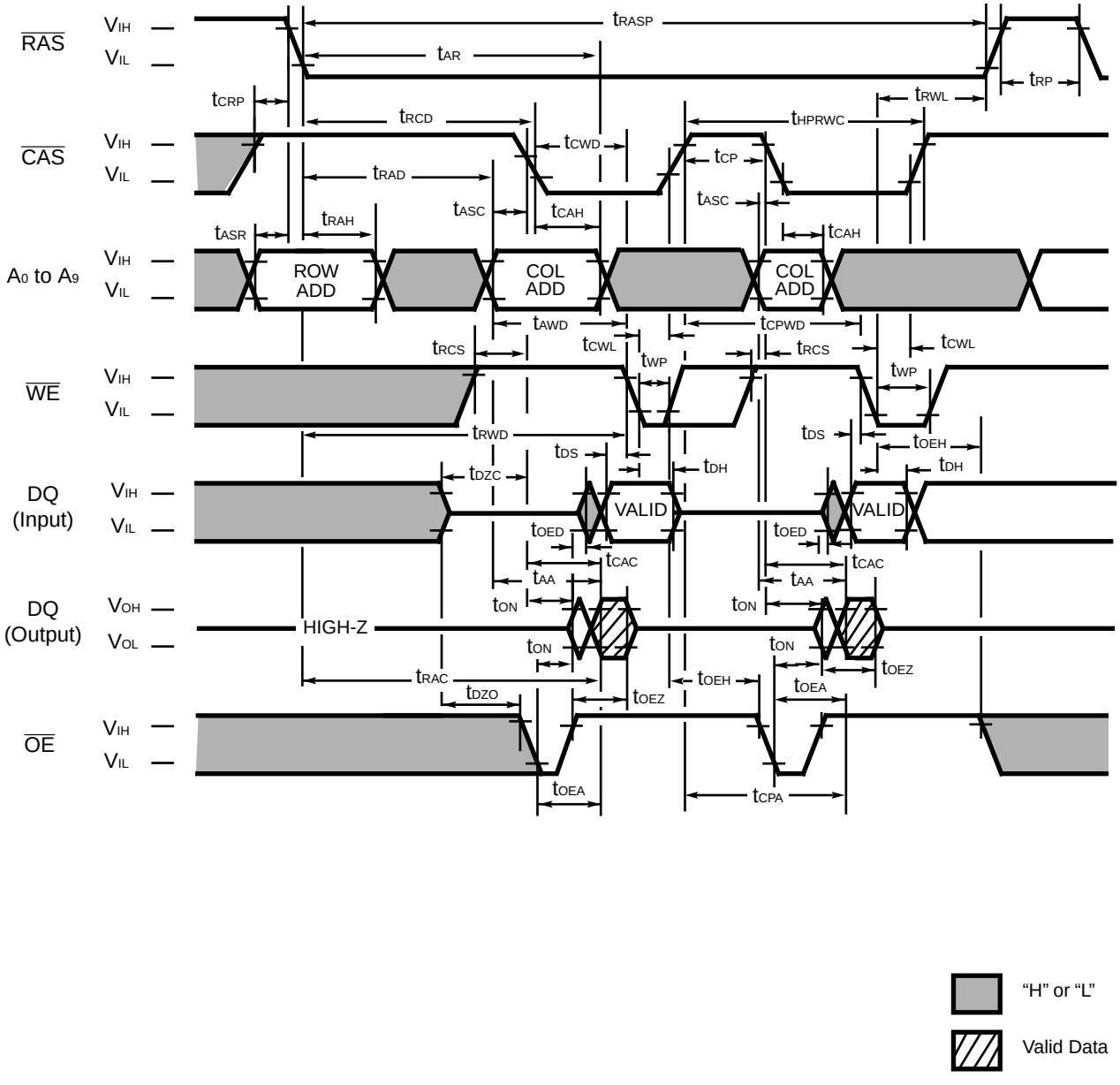
**Fig. 14 – HYPER PAGE MODE READ/WRITE MIXED CYCLE**




DESCRIPTION

The hyper page mode performs read/write operations repetitively during one $\overline{RAS}$ cycle. At this time, $t_{HPC}$ (min.) is invalid.

**Fig. 15 – HYPER PAGE MODE READ-MODIFY-WRITE CYCLE**

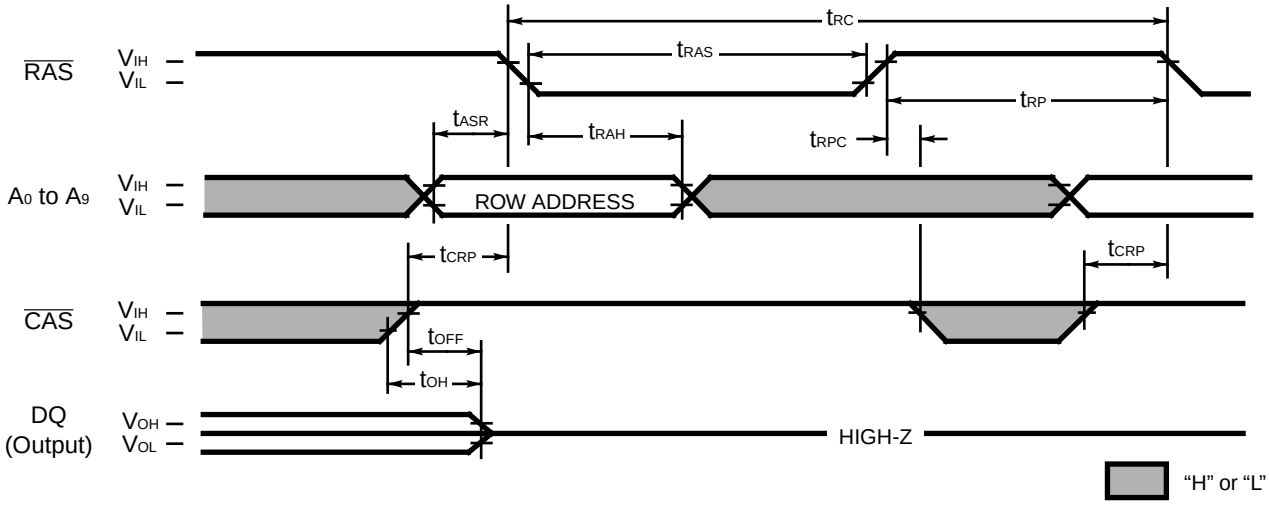



DESCRIPTION

During the hyper page mode of operation, the read-modify-write cycle can be executed by switching $\overline{WE}$ from High to Low after input data appears at the DQ pins during a normal cycle.

# MB81V4405C-60/MB81V4405C-70

**Fig. 16 – $\overline{RAS}$-ONLY REFRESH ($\overline{WE}$ = $\overline{OE}$ = "H" or "L")**

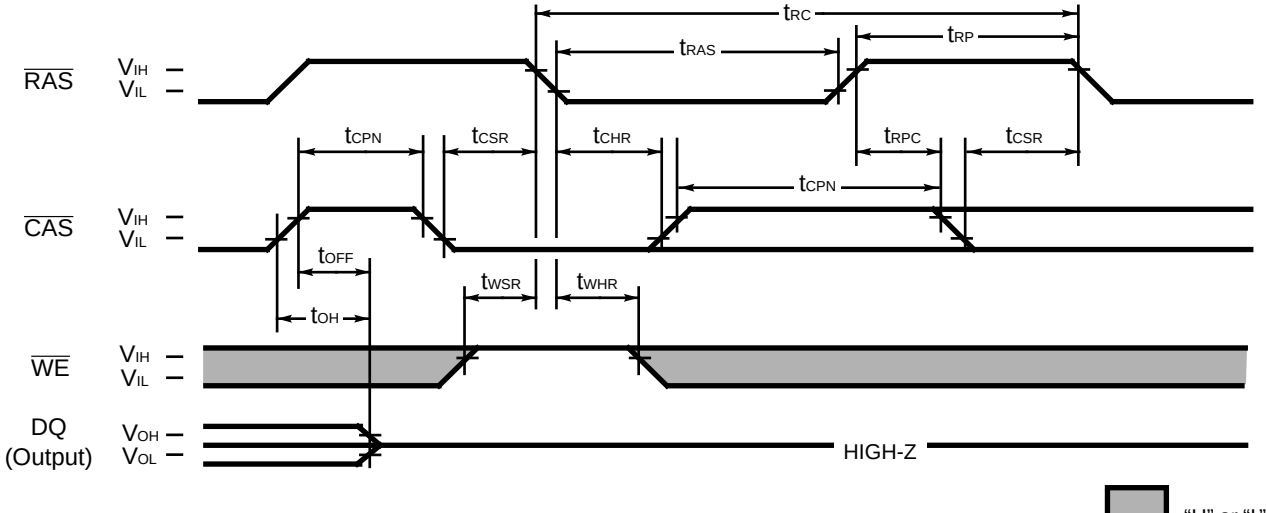



DESCRIPTION

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 1,024 row addresses every 16.4-milliseconds. Three refresh modes are available: $\overline{RAS}$-only refresh, $\overline{CAS}$-before-$\overline{RAS}$ refresh, and hidden refresh.

$\overline{RAS}$-only refresh is performed by keeping $\overline{RAS}$ Low and $\overline{CAS}$ High throughout the cycle; the row address to be refreshed is latched on the falling edge of $\overline{RAS}$. During $\overline{RAS}$-only refresh, DQ pins are kept in a high-impedance state.

**Fig. 17 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH (ADDRESSES = $\overline{OE}$ = "H" or "L")**

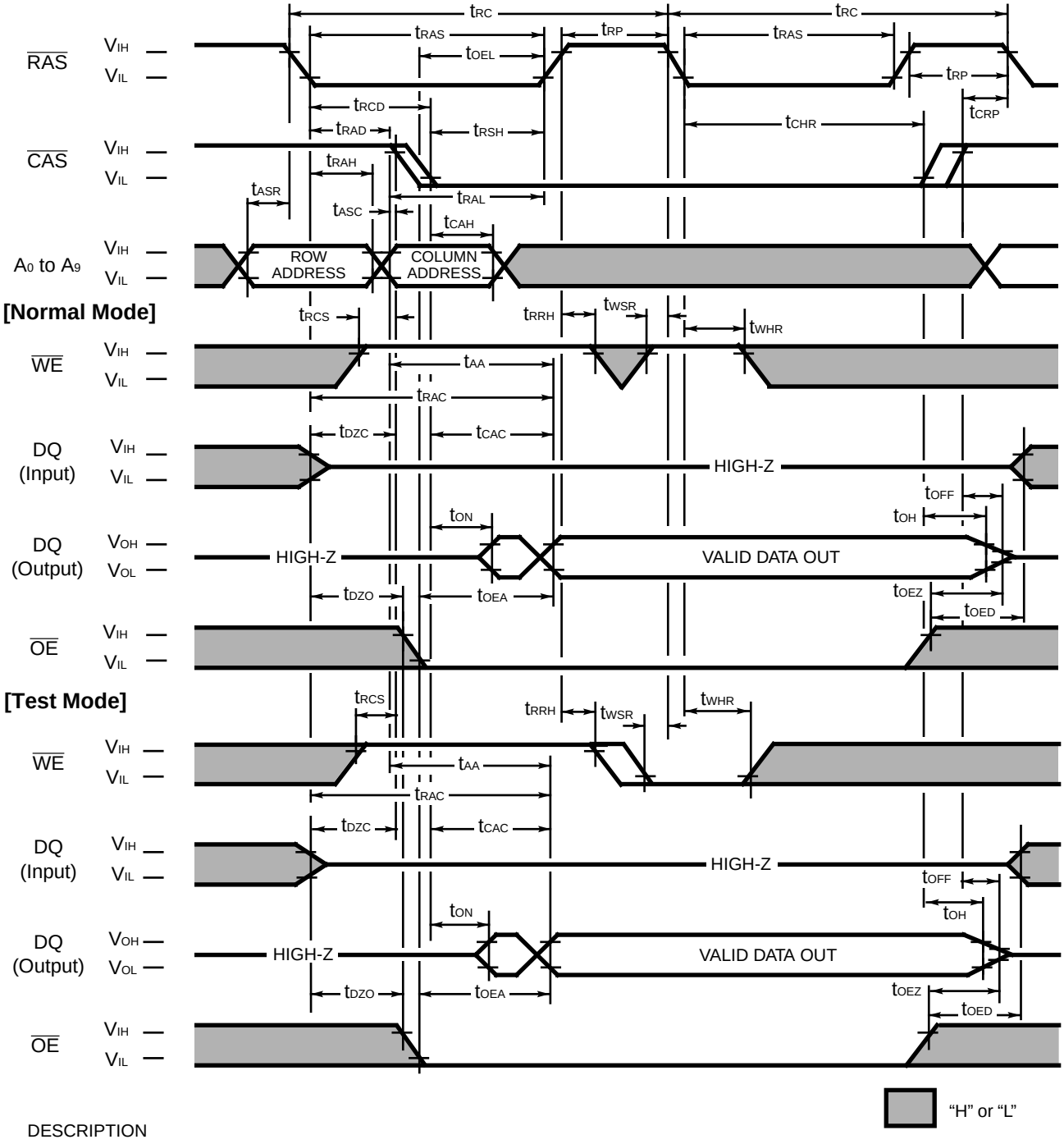



DESCRIPTION

$\overline{CAS}$-before-$\overline{RAS}$ refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held Low for the specified setup time ($t_{CSR}$) before $\overline{RAS}$ goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh operation.

$\overline{WE}$ must be held High for the specified set up time ($t_{WSR}$) before $\overline{RAS}$ goes Low in order not to enter "TEST MODE".

**Fig. 18 – HIDDEN REFRESH CYCLE**



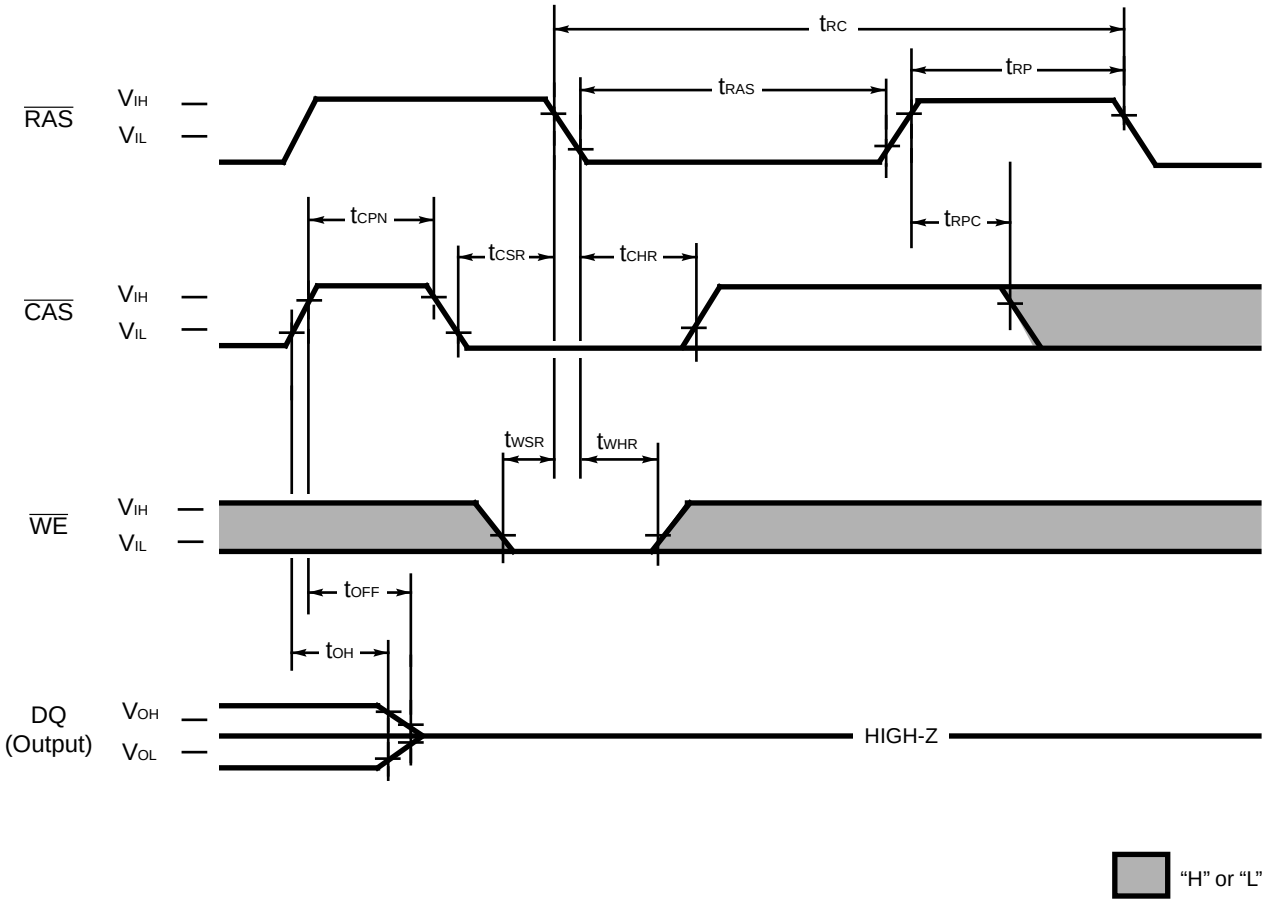

DESCRIPTION

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of $\overline{CAS}$ and cycling $\overline{RAS}$. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

$\overline{WE}$ must be held High for the specified set up time ($t_{WSR}$) before $\overline{RAS}$ goes Low in order not to enter "test mode".

# MB81V4405C-60/MB81V4405C-70

**Fig. 19 – TEST MODE SET CYCLE ($A_0$ to $A_9$, $\overline{OE}$ = "H" or "L")**




DESCRIPTION

Test Mode;

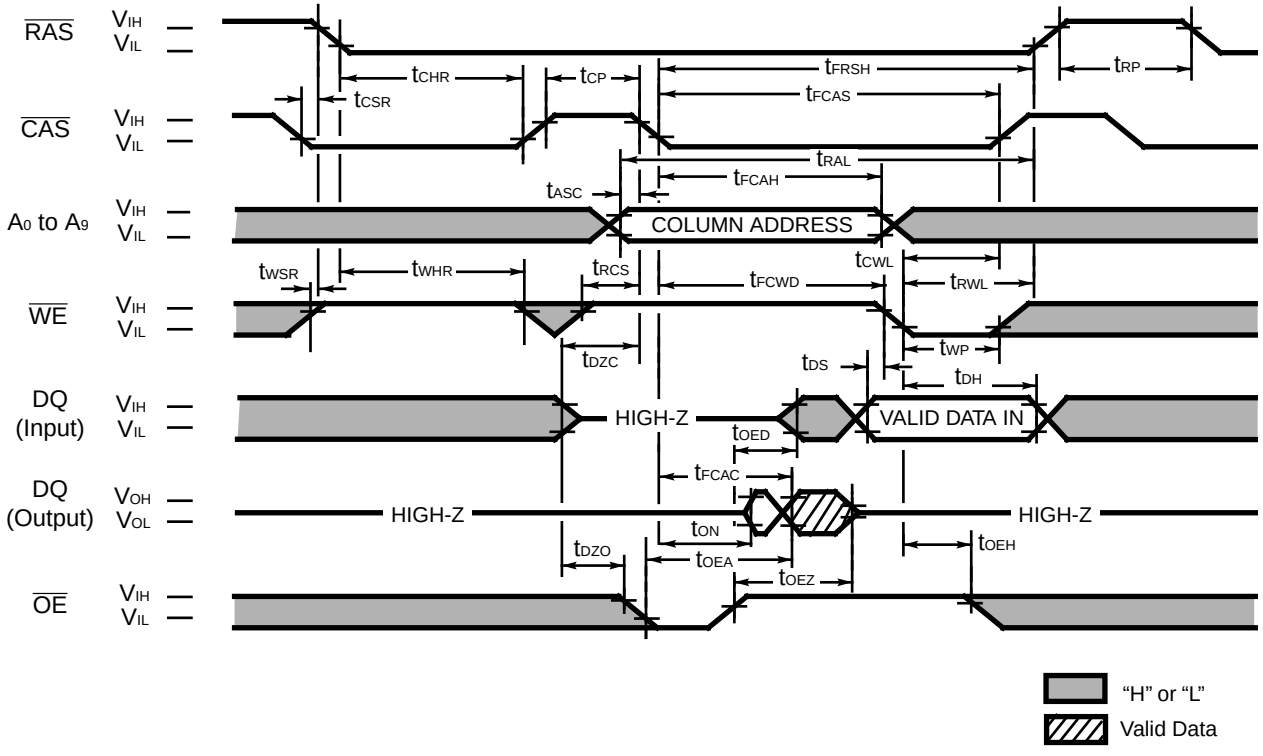
The purpose of this test mode is to reduce device test time to half of that required to test the device conventionally.
The test mode function is entered by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ (WCBR) refresh for the entry cycle.
In the test mode, read and write operations are executed in units of eights bits which are selected by the address combination of $CA_0$.
In the write mode, data is written into eight cells simultaneously. But the data must be input from all DQ pins. In the read mode, the data of eight cells at the selected addresses are read out from DQ and checked in the following manner.

When the eight bits are all "L" or all "H", a "H" level is output.
When the eight bits show a combination of "L" and "H", a "L" level is output.

The test mode function is exited by performing a $\overline{RAS}$-only refresh or a $\overline{CAS}$-before-$\overline{RAS}$ refresh for the exit cycle.
In test mode operation, the following parameters are delayed approximately 5 ns from the specified value in the data sheet.

$t_{RC}$, $t_{RWC}$, $t_{RAC}$, $t_{AA}$, $t_{RAS}$, $t_{CSH}$, $t_{RAL}$, $t_{RWD}$, $t_{AWD}$, $t_{PC}$, $t_{PRWC}$, $t_{CPA}$, $t_{RHCP}$, $t_{CPWD}$

**Fig. 20 – $\overline{CAS}$-BEFORE-$\overline{RAS}$ REFRESH COUNTER TEST CYCLE**




DESCRIPTION

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle provides a convenient method to verify the functionality of $\overline{CAS}$-before-$\overline{RAS}$ refresh circuitry. If, after a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle. $\overline{CAS}$ makes a transition from High to Low while $\overline{RAS}$ is held Low, read and write operations are enabled as shown above. Row and column addresses are defined as follows:

Row Address: Bits $A_0$ through $A_9$ are defined by the on-chip refresh counter.

Column Address: Bits $A_0$ through $A_9$ are defined by latching levels on $A_0$-$A_9$ at the second falling edge of $\overline{CAS}$.

The $\overline{CAS}$-before-$\overline{RAS}$ Counter Test procedure is as follows ;

1) Initialize the internal refresh address counter by using 8 $\overline{RAS}$ only refresh cycles.
2) Use the same column address throughout the test.
3) Write "0" to all 1024 row addresses at the same column address by using normal write cycles.
4) Read "0" written in procedure 3) and check; simultaneously write "1" to the same addresses by using $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test (read-modify-write cycles). Repeat this procedure 1024 times with addresses generated by the internal refresh address counter.
5) Read and check data written in procedure 4) by using normal read cycle for all 1024 memory locations.
6) Reverse test data and repeat procedures 3), 4), and 5).

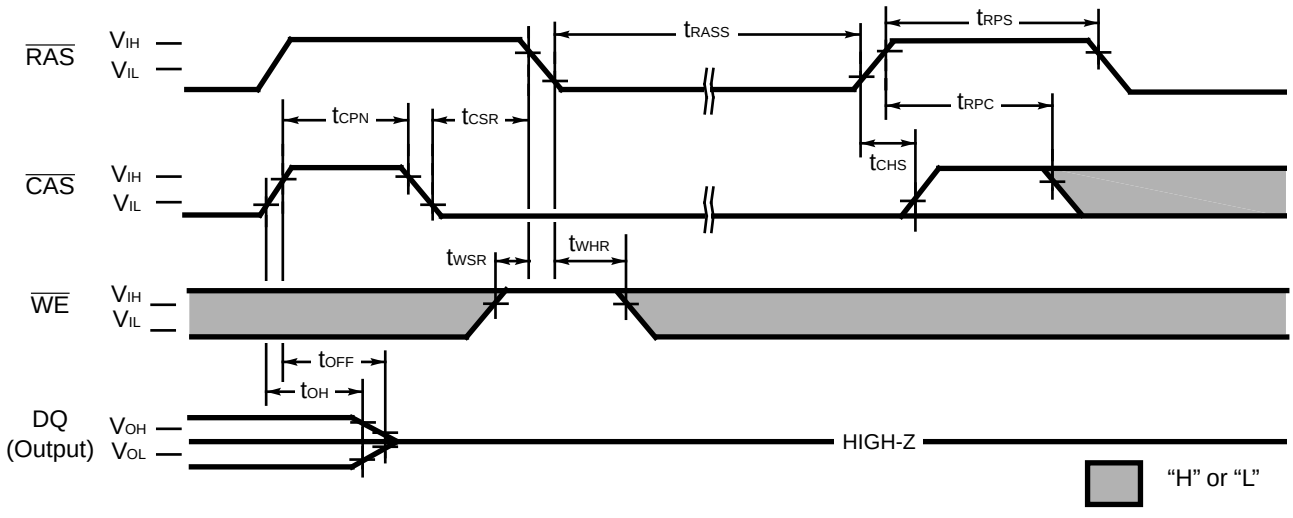
**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Symbol | MB81V4405C-60 | | MB81V4405C-70 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| 90 | Access Time from $\overline{CAS}$ | $t_{FCAC}$ | — | 35 | — | 40 | ns |
| 91 | Column Address Hold Time | $t_{FCAH}$ | 30 | — | 30 | — | ns |
| 92 | $\overline{CAS}$ to $\overline{WE}$ Delay Time | $t_{FCWD}$ | 55 | — | 60 | — | ns |
| 93 | $\overline{CAS}$ Pulse Width | $t_{FCAS}$ | 35 | — | 40 | — | ns |
| 94 | $\overline{RAS}$ Hold Time | $t_{FRSH}$ | 35 | — | 40 | — | ns |

Note: Assumes that $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle only.

# MB81V4405C-60/MB81V4405C-70

**Fig. 21 – SELF REFRESH CYCLE ($A_0$ - $A_9$ = $\overline{OE}$ = "H" or "L")**




**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Symbol | MB81V4405C-60 | | MB81V4405C-70 | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Max. | Min. | Max. | |
| 100 | $\overline{RAS}$ Pulse Width | $t_{RASS}$ | 100 | — | 100 | — | µs |
| 101 | $\overline{RAS}$ Precharge Time | $t_{RPS}$ | 104 | — | 119 | — | ns |
| 102 | $\overline{CAS}$ Hold Time | $t_{CHS}$ | –50 | — | –50 | — | ns |

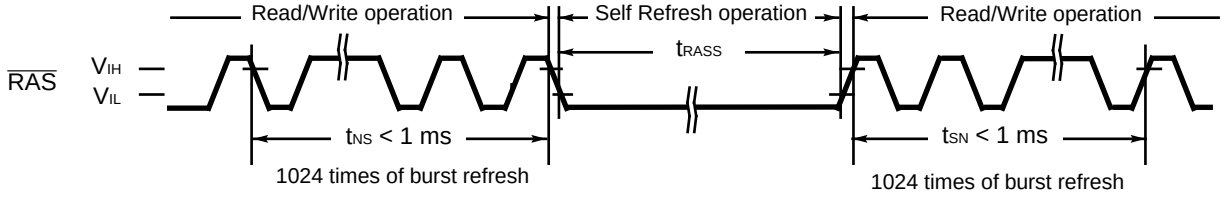
Note: Assumes self refresh cycle only

DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter.
If $\overline{CAS}$ goes to "L" before $\overline{RAS}$ goes to "L" (CBR) and the condition of $\overline{CAS}$ "L" and $\overline{RAS}$ "L" is kept for term of $t_{RASS}$ (more than 100 µs), the device can be entered the self refresh cycle. And after that, refresh operation is automatically executed per fixed interval using internal refresh address counter during "$\overline{RAS}$ = L" and "$\overline{CAS}$ = L".
And exit from self refresh cycle is performed by toggling of $\overline{RAS}$ and $\overline{CAS}$ to "H" with specifying $t_{CHS}$ min..

Restruction for Self refresh operation;
For self refresh operation, the notice below must be considered.

1) In the case that distribute CBR refresh are operated in read/write cycles
   Self refresh cycles can be executed without special rule if 1024 cycles of distribute CBR refresh are executed within $t_{REF}$ max..
2) In the case that burst CBR refresh or $\overline{RAS}$ only refresh are operated in read/write cycles
   1024 times of burst CBR refresh or 1024 times of burst $\overline{RAS}$ only refresh must be executed before and after Self refresh cycles.

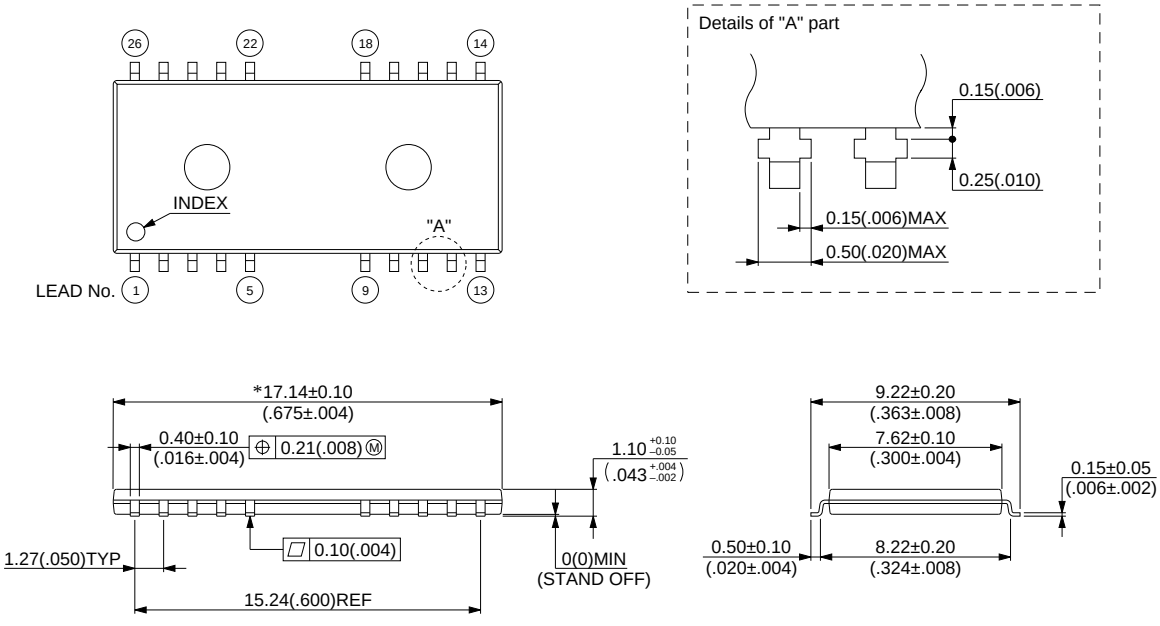


## ■ PACKAGE DIMENSIONS

(Suffix: -PFTN)

26 pin, Plastic TSOP(II)
(FPT-26P-M01)

* : This dimension includes resin protrusion.(Each side : 0.15(.006) MAX)




Dimensions in mm (inches).

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